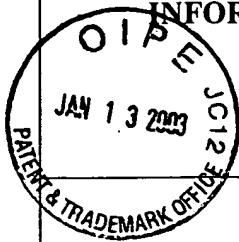


#10



INFORMATION DISCLOSURE STATEMENT

BY APPLICANT

Docket: 1011-54375

App: 09/620,021

Applicant: Rajski et al.

Filed: July 20, 2000

Art Unit: 2133

U.S. PATENT DOCUMENTS

Init.*	Number	Date	Name	Class	Sub	Filed
	6,300,885 B1	10/9/01	Davenport et al.			RECEIVED JAN 14 2003

OTHER DOCUMENTS

Technology Center 2100

pme			P.H. Bardell, W.H. McAnney, J. Savir, "Built in test for VLSI: Pseudorandom Techniques, John Wiley & Sons, 1987.
pme			W.B. Jone and S.R. Das, "Space compression method for built-in self testing of VLSI circuits," <i>Int. Journal of Computer Aided VLSI Design</i> , vol. 3, pp. 309-322, 1991.
pme			H.J. Wunderlich, "On computing optimized input probabilities for random tests," <i>Proc. DAC</i> pp. 392-398, 1987.
pme			N.R. Saxena and J.P. Robinson, "Accumulator compression testing," <i>IEEE Trans. Comput.</i> , vol. C-35, No. 4, pp. 317-321, 1986.
pme			J.P. Hayes, "Check sum test methods," <i>Proc. FTCS</i> , pp. 114-120, 1976.
pme			J. Savir, "Syndrome-testable design of combinational circuits," <i>IEEE Trans. Comput.</i> Vol. C-29, No. 6, pp. 442-451, 1980.
pme			Y.K. Li and J.P. Robinson, "Space compression methods with output data modification," <i>IEEE Trans. CAD of Integrated Circuits and Systems</i> , vol. CAD-6, No. 2, pp. 290-294, 1987.
pme			J.E. Smith, "Measures of the effectiveness of fault signature analysis," <i>IEEE Trans. Comput.</i> , vol. C-29, No. 6, pp. 510-514, 1980.

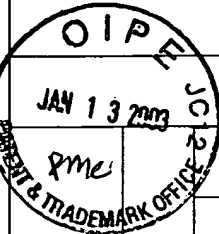
EXAMINER:

Phung My Chung

DATE

3/12/03

*Examiner: Initial if considered, whether or not in conformance with MPEP 609; draw line through cite if not in conformance and not considered. Send copy.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Docket: 1011-54375	App: 09/620,021
		Applicant: Rajski et al.	
		Filed: July 20, 2000	Art Unit: 2133
OTHER DOCUMENTS			
		K.J. Latawiec, "New method of generation of shifted linear pseudorandom binary sequences", <i>Proc. IEE</i> , vol. 121, No. 8, pp. 905-906, 1974	RECEIVED JAN 14 2003 Technology Center 2100
		N.R. Saxena and E.J. McCluskey, "Extended precision checksums," <i>Proc. FTCS</i> , pp. 142-147, 1987.	
		J.P. Hayes, "Transition count testing of combinational logic circuits," <i>IEEE Trans. Comput.</i> , vol. C-25, No. 6, pp. 613-620, 1976.	
		P.H. Bardell and W.H. McAnney, "Pseudorandom arrays for built-in tests," <i>ISSS Trans. Comput.</i> , vol. C-35, No. 7, pp. 653-658, 1986.	
		B. Ireland and J.E. Marshall, "Matrix method to determine shift-register connections for delayed pseudorandom binary sequences," <i>Electronics Letters</i> , vol. 4 No. 15, pp. 309-310, 1968.	
		J.A. Waicukauski, E. Lindbloom, E.B. Eichelberger and O.P. Forlenza, "A method for generating weighted random test patterns," <i>IBM J. Res. Develop.</i> , vol. 33, no. 2, pp. 149-161, March 1989	
		R.A. Frohwerk, "Signature analysis: a new digital field services method," <i>Hewlett-Packard Journal</i> , pp. 2-8, May 1997.	
		G. Hetherington, T. Fryars, N. Tamarapalli, M. Kassab, A. Hasson and J. Rajski, "Logic BIST for Large Industrial Designs: Real Issues and Case Studies," <i>Proc. ITC</i> , pp. 358-367, 1999.	
	V. Iyengar, K. Chakrabarty and B.T. Murray, "Built-In Self-testing of sequential circuits using precomputed test sets," <i>Proc. VLSI Test Symposium</i> , pp. 418-423, 1998.		
EXAMINER: <u>Phung Chung</u>		DATE <u>3/12/03</u>	
*Examiner: Initial if considered, whether or not in conformance with MPEP 609; draw line through cite if not in conformance and not considered. Send copy.			

INFORMATION DISCLOSURE STATEMENT

BY APPLICANT

Docket: 1011-54375

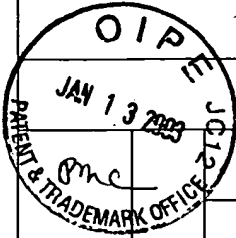
App: 09/620,021

Applicant: Rajski et al.

Filed: July 20, 2000

Art Unit: 2133

OTHER DOCUMENTS



A. Jas, J. Ghosh-Dastidar and N.A. Touba, "Scan vector compression/decompression using statistical coding," Proc. VLSI Test Symposium, pp. 114-120, 1999.

RECEIVED

JAN 14 2003

Technology Center 2100

A.Jas and N.A. Touba, "Test vector decompression via cyclical scan chains and its application to testing core-based designs," Proc. ITC, pp.458-464, 1998.

EXAMINER:

Phung Chung

DATE

3/12/03

*Examiner: Initial if considered, whether or not in conformance with MPEP 609; draw line through cite if not in conformance and not considered. Send copy.

INFORMATION DISCLOSURE STATEMENT

BY APPLICANT

Docket: 1011-54375

App: 09/620,021

Applicant: Rajski et al.

Filed: July 20, 2000

Art Unit: 2133

RECEIVED

OTHER DOCUMENTS

JAN 14 2003

M. Serra, T. Slater, J.C. Muzio and D.M. Miller, "The analysis of one-dimensional linear cellular automata and their aliasing properties," *IEEE Trans. CAD of Integrated Circuits and Systems*, vol. CAD-9, No. 7, pp. 767-778, 1990.

T.W. Williams, W. Daehn, M. Gruetzner and C.W. Starke, "Bounds and analysis of aliasing errors in linear-feedback shift registers," *IEEE Trans. CAD of Integrated Circuits and Systems*, vol. CAD-7, No. 1, pp. 75-83, 1988.

M. Ishida, D.S. Ha and T. Yamaguchi, "COMPACT: A hybrid method for compression test data," *Proc. VLSI Test Symposium*, pp. 62-69, 1998.

K. Kim, D.S. Ha and J.G. Tront, "On using signature registers as pseudorandom pattern generators in built-in self testing," *IEEE Trans. CAD of IC*, vol. CAD-7, No. 8, 1988, pp.919-928.

G. Mrugalski, J. Rajski and J. Tyszer, "Synthesis of pattern generators based on cellular automata with phase shifters," *Proc. Int. Test Conf.*, pp. 368-377, 1999.

R. Kapur, S. Patil, T.J. Snethen and T.W. Williams, "Design of an efficient weighted random pattern generation system," *Proc. ITC.*, pp. 491-500, 1994.

F. Muradali, V.K. Agarwal and B. Nadeau-Dostie, "A new procedure for weighted random built-in self-test," *Proc. ITC.*, pp. 600-669, 1990.

S. Pateras and J. Rajski, "Cube contained random patterns and their application to the complete testing of synthesized multi-level circuits," *Proc. ITC.*, pp. 473-482, 1991.

J. Rajski and J. Tyszer, "Test responses compaction in accumulators with rotate carry adders," *IEEE Transactions CAD of Integrated Circuits and Systems*, vol. CAD-12, No. 4, pp. 531-539, 1993.

EXAMINER:

Phung Chung

DATE

3/12/03

*Examiner: Initial if considered, whether or not in conformance with MPEP 609; draw line through cite if not in conformance and not considered. Send copy.

INFORMATION DISCLOSURE STATEMENT

BY APPLICANT

Docket: 1011-54375

App: 09/620,021

Applicant: Rajski et al.

Filed: July 20, 2000

Art Unit: 2533

JAN 14 2003

OTHER DOCUMENTS

Technology Center 2100

J. Rajski and J. Tyszer, "Accumulator-based compaction of test responses," *IEEE Transactions on Comput.*, vol. C-42, No. 6, pp. 643-650, 1993.

N.R. Saxena and E.J. McCluskey, "Analysis of checksums, extended-precision checksums, and cyclic redundancy," *IEEE Trans. Comput.*, vol. C-39, No. 7, pp. 969-975, 1990.

N.A. Toubia and E.J. McCluskey, "Transformed pseudo-random patterns for BIST," *Proc. VLSI Test Symposium*, pp. 410-416, 1995.

N.A. Toubia and E.J. McCluskey, "Altering a pseudo-random bit sequence for scan-based BIST," *Proc. ITC.*, pp. 167-175, 1996.

K.H. Tsai, S. Hellebrand, J. Rajski and Marek-Sadowska, "STARBIST: Scan autocorrelated random pattern generation," *Proc. DAC*, pp. 472-477, 1997.

H.J. Wunderlich and G. Kiefer, "Bit-flipping BIST," *Proc. ICCAD*, pp. 337-343, 1996.

S.W. Golomb, *Shift Register Sequences*, Holden Day, San Francisco, 1967.

V.N. Yarmolik and S.N. Demidenko, "Generation and Application of Pseudorandom Sequences for Random Testing," J. Wiley & Sons, New York, 1988.

EXAMINER: *Phung Chung*DATE *3/12/03*

*Examiner: Initial if considered, whether or not in conformance with MPEP 609; draw line through cite if not in conformance and not considered. Send copy.